MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2016/2017

EEE4186 - VLSI SYSTEM DESIGN AND MODELING TECHNIQUE

(EE)

24 FEBRUARY 2017
9:00 AM – 11:00 AM
(2 Hours)

INSTRUCTION TO STUDENTS

1. This Question paper consists of **5 pages** including cover page with **4 Questions** only.

2. Attempt **ALL FOUR** questions. All questions carry equal marks and the distribution of the marks for each question is the same.

3. Please print all your answers in the answer Booklet provided.

4. **A VHDL model** means an entity-architecture pair, plus any extra codes that might be necessary for them to work properly (library, use, etc.)

5. When names (of entities, architectures, signals, etc.) are not specified, you may use any suitable and valid name.

Question 1

(a) Sketch the flow of four abstraction level in VHDL and briefly describe each level.
[5 marks]

(b) Figure Q1 shows the circuit diagram of a bit-serial adder, which consists of a full-adder and a D-flip-flop.

(i) Construct the ***entity*** of this circuit using entity name: *serial_adder*.
[3 marks]

(ii) Write the ***architecture*** of this circuit using VHDL structural code by instantiate ***component*** *full_adder* and *D_flip_flop*. Use architecture name: *structural*.
[9 marks]

(iii) Construct the complete VHDL RTL code for the *D_flip_flop* in this circuit. The **reset** is an active-low signal. Do not use logic gate.
[8 marks]

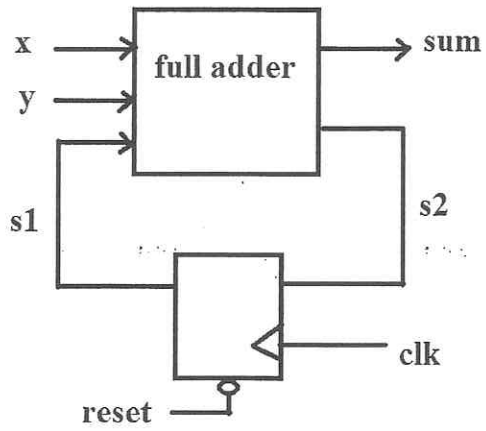

Figure Q1

Continued ...

Question 2

(a) Sketch the logic circuit diagram for the synthesized VHDL code shown in Figure Q2a.

[12 marks]

```
entity circuit is
port (d1,d2,d3,d4,d5,d6    : in  std_logic;
      dout_1,dout_2,dout_3: out std_logic);
end circuit;

architecture logic of circuit is
begin
      dout_1 <= (d1 nand not d2) or (d2 nand d3);
      dout_2 <= (d3 nand d4) nand (d3 xor d5);
      dout_3 <= ((d3 nand d4) and d5) nor d6;
end logic;
```

Figure Q2a

(b) Figure Q2b shows the logic diagram for a subtractor to perform subtraction of two input vector, A and B. Create a ***function*** that subtracts std_logic_vectors and returns the result. Call your function ***minus***. The ***function*** must accept std_logic_vectors of any size. For simplicity, assume that the two operands (A and B vectors) are same size. Contain your ***function*** inside a new ***package*** called ***my_package.***

[13 marks]

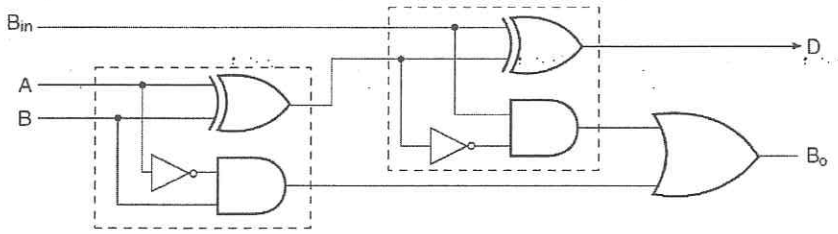

Figure Q2b

Continued ...

Question 3

(a) A truth table of an arithmetic circuit is shown in Figure Q3a below. Input ***A*** and ***B*** are 8-bits data, ***S*** is 2-bits select signal, and ***Dout*** is 8-bits output signal. Sketch the circuit diagram for the arithmetic circuit using 4-to-1 multiplexer and standard logic gates.

[6 marks]

S	*Operation*
00	*NOT A*
01	*A OR B*
10	*A XOR B*
11	*A AND B*

Figure Q3a

(b) Write complete VHDL RTL code for the circuit in part (a) above. Name the entity as *arithmetic*. Use:
(i) Selected Signal Assignment
(ii) ***case*** statement

[12 marks]

(c) Create a test-bench in VHDL code to test the circuit in part (a), by referring to the work.arithmetic(beh). Test the circuit in part (a) using the test-bench input signals shown in Figure Q3b by referring to the time step in the diagram.

[7 marks]

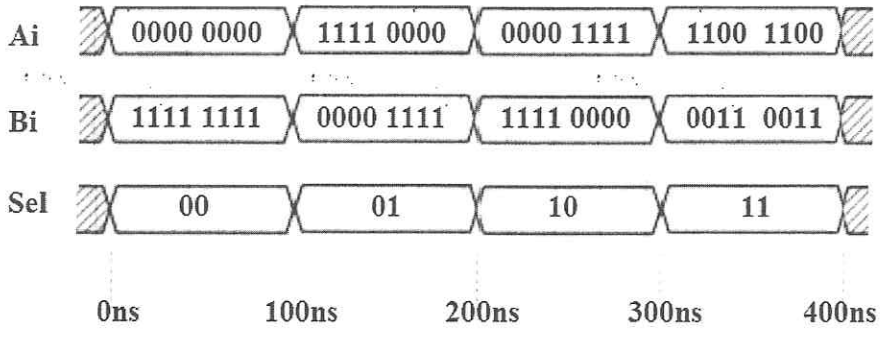

Figure Q3b

Continued ...

Question 4

(a) Create and write the complete VHDL RTL code for the Moore finite state machine (FSM) shown in Figure Q4a. Use separate ***process*** statement for combinational and sequential logic. Note that **Reset** is asynchronous reset signal, **w** is the input signal and **z** is the output signal.

[18 marks]

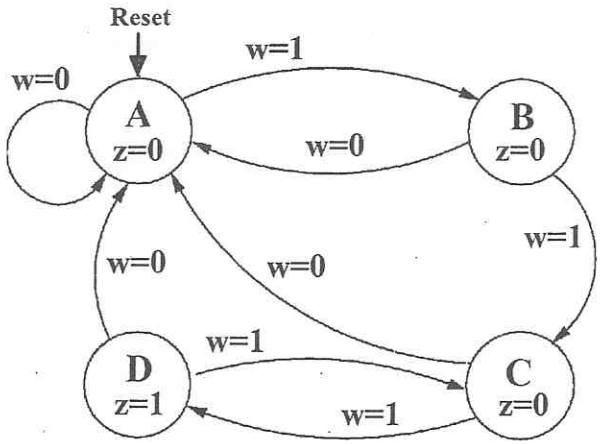

Figure Q4a

(b) The FSM in (a) is modified into Mealy FSM as per Figure Q4b. Re-write only the output stage of the VHDL code for Figure Q4b.

[7 marks]

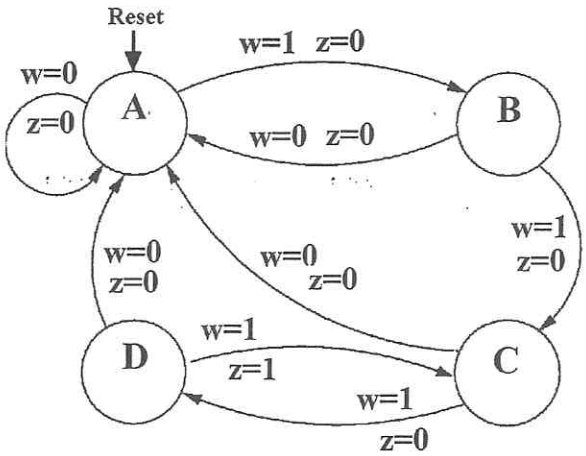

Figure Q4b

End of Paper